## Claims

We claim the following invention:

1. A System-on-Chip (SOC) interconnection apparatus, comprising:

a single semiconductor integrated circuit that includes one or more requestors and one or more addressable targets, wherein each said addressable target has a unique address space and further comprises one or more of the following: resident memory, a memory controller for resident or off-chip memory, an addressable bridge to a device, an addressable bridge to a system, or an addressable bridge to a sub-system;

an internal switching fabric that routes signals between said requestors and said addressable targets, said internal switching fabric further comprises one or more decoder/router elements, wherein each decoder/router element receives a request from a requestor, determines which said addressable target is the designated target using an internal system memory map, and routes said request to said designated target;

one or more requestor connection ports, wherein each said connection port connects one of said requestors to said internal switching fabric; and

one or more target connection ports, wherein each said target port connects one of said addressable targets to said internal switching fabric.

2. A system that includes a System-on-Chip (SOC) having an interconnection apparatus comprising:

a single semiconductor integrated circuit that includes one or more requestors and one or more addressable targets, wherein each said addressable target has a unique address space and further comprises one or more of the following: resident memory, a memory controller for resident or off-chip memory, an addressable bridge to

a device, an addressable bridge to a system, or an addressable bridge to a sub-system;

an internal switching fabric that routes signals between said requestors and said addressable targets, said internal switching fabric further comprises one or more decoder/router elements, wherein each decoder/router element receives a request from a requestor, determines which said addressable target is the designated target using an internal system memory map, and routes said request to said designated target;

one or more requestor connection ports, wherein each said connection port connects one of said requestors to said internal switching fabric; and

one or more target connection ports, wherein each said target port connects one of said addressable targets to said internal switching fabric.

3. A method to make a System-on-Chip (SOC) interconnection apparatus, comprising:

providing a single semiconductor integrated circuit that includes one or more requestors and one or more addressable targets, wherein each said addressable target has a unique address space and further comprises one or more of the following: resident memory, a memory controller for resident or off-chip memory, an addressable bridge to a device, an addressable bridge to a system, or an addressable bridge to a subsystem;

coupling an internal switching fabric to said addressable targets and said requestors, said internal switching fabric routes signals between said requestors and said addressable targets, said internal switching fabric further comprises one or more decoder/router elements, wherein each decoder/router element receives a request from a requestor, determines which said addressable target is the designated target using an

internal system memory map, and routes said request to said designated target;

providing one or more requestor connection ports, wherein each said connection port connects one of said requestors to said internal switching fabric; and

providing one or more target connection ports, wherein each said target port connects one of said addressable targets to said internal switching fabric.

4. A method to use a System-on-Chip (SOC) interconnection apparatus, comprising:

receiving a request from one of one or more requestors over a requestor connection port coupled to said one requestor and to an internal switching fabric;

determining which one of one or more addressable targets is the designated target using an internal system memory map; and

routing said request to said designated target over a target connection port coupled to said internal switching fabric;

wherein said internal switching fabric, said one or more requestors, and said one or more addressable targets are all included on a single semiconductor integrated circuit, wherein each said addressable target has a unique address space and further comprises one or more of the following: resident memory, a memory controller for resident or off-chip memory, an addressable bridge to a device, an addressable bridge to a system, or an addressable bridge to a subsystem, and wherein said internal switching fabric routes signals between said requestors and said addressable targets and further comprises one or more decoder/router elements that receive said request from a requestor.

5. A program storage device readable by a computer that tangibly embodies a program of instructions executable by the computer to perform a method to use a System-on-Chip (SOC) interconnection apparatus, said method comprising:

receiving a request from one of one or more requestors over a requestor connection port coupled to said one requestor and to an internal switching fabric;

determining which one of one or more addressable targets is the designated target using an internal system memory map; and

routing said request to said designated target over a target connection port coupled to said internal switching fabric;

wherein said internal switching fabric, said one or more requestors, and said one or more addressable targets are all included on a single semiconductor integrated circuit, wherein each said addressable target has a unique address space and further comprises one or more of the following: resident memory, a memory controller for resident or off-chip memory, an addressable bridge to a device, an addressable bridge to a system, or an addressable bridge to a subsystem, and wherein said internal switching fabric routes signals between said requestors and said addressable targets and further comprises one or more decoder/router elements that receive said request from a requestor.

6. A dependent claim according to claim 1, 2, 3, 4, or 5, wherein said internal switching fabric further comprises one or more arbiters.

7. A dependent claim according to claim 1, 2, 3, 4, or 5, wherein one of said one or more decoder/router elements further comprises one of the following:

a decoder/router element that routes requests to all of said one or more addressable targets using an internal system memory map that includes unique address space information for all of said one or more addressable targets;

a decoder/router element that routes requests to less than all of said one or more addressable targets using an internal system memory map that includes unique address space information for all of said one or more addressable targets; or

a decoder/router element that routes requests to less than all of said one or more addressable targets using an internal system memory map that includes unique address space information for less than all of said one or more addressable targets.

8. A dependent claim according to claim 1, 2, 3, 4, or 5, wherein one of said one or more requestors and one of said one or more addressable targets together further comprise a single device having an independently accessible requestor port and an independently accessible target port.

9. A dependent claim according to claim 1, 2, 3, 4, or 5, wherein one of said one or more addressable targets further comprises a single device having two independently accessible target ports.

10. A dependent claim according to claim 1, 2, 3, 4, or 5, wherein said request routed to said designated target by said decoder/router element further comprises a registered, point-to-point signal that further comprises a plurality of pipeline stages.

11. A System-on-Chip (SOC) interconnection apparatus, comprising:

a single semiconductor integrated circuit that includes one or more requestors and one or more addressable targets, wherein each said addressable target has a unique address space and further comprises one or more of the following: resident memory, a memory controller for resident or off-chip memory, an addressable bridge to a device, an addressable bridge to a system, or an addressable bridge to a subsystem;

an internal switching fabric that routes signals between said requestors and said addressable targets, said internal switching fabric further comprises one or more decoder/router elements and one or more arbiters, wherein each decoder/router element receives a request from a requestor, determines which said addressable target is the designated target using an internal system memory map, and routes said request to said designated target, wherein said request routed to said designated target further comprises a registered, point-to-point signal having a plurality of pipeline stages;

one or more requestor connection ports, wherein each said connection port connects one of said requestors to said internal switching fabric; and

one or more target connection ports, wherein each said target port connects one of said addressable targets to said internal switching fabric;

wherein one of said one or more decoder/router elements further comprises one of the following:

a decoder/router element that routes requests to all of said one or more addressable targets using an internal system memory map that includes unique address space information for all of said one or more addressable targets;

a decoder/router element that routes requests to less than all of said one or more addressable targets using an internal system memory map that includes unique address space information for all of said one or more addressable targets; or

a decoder/router element that routes requests to less than all of said one or more addressable targets using an internal system memory map that includes unique address space information for less than all of said one or more addressable targets; and

wherein one of said one or more requestors and one of said one or more addressable targets together further comprise a single device having an independently accessible requestor port and an independently accessible target port; or

one of said one or more addressable targets further comprises a single device having two independently accessible target ports.

12. A system that includes a System-on-Chip (SOC) having an interconnection apparatus comprising:

a single semiconductor integrated circuit that includes one or more requestors and one or more addressable targets, wherein each said addressable target has a unique address space and further comprises one or more of the following: resident memory, a memory controller for resident or off-chip memory, an addressable bridge to a device, an addressable bridge to a system, or an addressable bridge to a subsystem;

an internal switching fabric that routes signals between said requestors and said addressable targets, said internal switching fabric further comprises one or more

decoder/router elements and one or more arbiters, wherein each decoder/router element receives a request from a requestor, determines which said addressable target is the designated target using an internal system memory map, and routes said request to said designated target, wherein said request routed to said designated target further comprises a registered, point-to-point signal having a plurality of pipeline stages;

one or more requestor connection ports, wherein each said connection port connects one of said requestors to said internal switching fabric; and

one or more target connection ports, wherein each said target port connects one of said addressable targets to said internal switching fabric;

wherein one of said one or more decoder/router elements further comprises one of the following:

a decoder/router element that routes requests to all of said one or more addressable targets using an internal system memory map that includes unique address space information for all of said one or more addressable targets;

a decoder/router element that routes requests to less than all of said one or more addressable targets using an internal system memory map that includes unique address space information for all of said one or more addressable targets; or

a decoder/router element that routes requests to less than all of said one or more addressable targets using an internal system memory map that includes unique address space information for less than all of said one or more addressable targets; and

wherein one of said one or more requestors and one of said one or more addressable targets together further comprise a single device having an independently accessible requestor port and an independently accessible target port; or

one of said one or more addressable targets further comprises a single device having two independently accessible target ports.

13. A method to make a System-on-Chip (SOC) interconnection apparatus, comprising:

providing a single semiconductor integrated circuit that includes one or more requestors and one or more addressable targets, wherein each said addressable target has a unique address space and further comprises one or more of the following: resident memory, a memory controller for resident or off-chip memory, an addressable bridge to a device, an addressable bridge to a system, or an addressable bridge to a subsystem;

providing an internal switching fabric that routes signals between said requestors and said addressable targets, said internal switching fabric further comprises one or more decoder/router elements and one or more arbiters, wherein each decoder/router element receives a request from a requestor, determines which said addressable target is the designated target using an internal system memory map, and routes said request to said designated target, wherein said request routed to said designated target further comprises a registered, point-to-point signal having a plurality of pipeline stages;

providing one or more requestor connection ports, wherein each said connection port connects one of said requestors to said internal switching fabric; and

providing one or more target connection ports, wherein each said target port

connects one of said addressable targets to said internal switching fabric;

wherein one of said one or more decoder/router elements further comprises one of the following:

a decoder/router element that routes requests to all of said one or more addressable targets using an internal system memory map that includes unique address space information for all of said one or more addressable targets;

a decoder/router element that routes requests to less than all of said one or more addressable targets using an internal system memory map that includes unique address space information for all of said one or more addressable targets; or

a decoder/router element that routes requests to less than all of said one or more addressable targets using an internal system memory map that includes unique address space information for less than all of said one or more addressable targets; and

wherein one of said one or more requestors and one of said one or more addressable targets together further comprise a single device having an independently accessible requestor port and an independently accessible target port; or

one of said one or more addressable targets further comprises a single device having two independently accessible target ports.

14. A method to use a System-on-Chip (SOC) interconnection apparatus, comprising:

receiving a request from one of one or more requestors over a requestor

connection port coupled to said one requestor and to an internal switching fabric;

determining which one of one or more addressable targets is the designated target using an internal system memory map; and

routing said request to said designated target over a target connection port coupled to said internal switching fabric, wherein said request routed to said designated target further comprises a registered, point-to-point signal having a plurality of pipeline stages;

wherein said internal switching fabric, said one or more requestors, and said one or more addressable targets are all included on a single semiconductor integrated circuit, wherein each said addressable target has a unique address space and further comprises one or more of the following: resident memory, a memory controller for resident or off-chip memory, an addressable bridge to a device, an addressable bridge to a system, or an addressable bridge to a subsystem, and wherein said internal switching fabric routes signals between said requestors and said addressable targets and further comprises one or more arbiters and one or more decoder/router elements that receive said request from a requestor;

wherein one of said one or more decoder/router elements further comprises one of the following:

a decoder/router element that routes requests to all of said one or more addressable targets using an internal system memory map that includes unique address space information for all of said one or more addressable targets;

a decoder/router element that routes requests to less than all of said one or more addressable targets using an internal system memory map that includes unique address space information for all of said one or more addressable targets; or

a decoder/router element that routes requests to less than all of said one or more addressable targets using an internal system memory map that includes unique address space information for less than all of said one or more addressable targets; and

wherein one of said one or more requestors and one of said one or more addressable targets together further comprise a single device having an independently accessible requester port and an independently accessible target port; or

one of said one or more addressable targets further comprises a single device having two independently accessible target ports.

15. A program storage device readable by a computer that tangibly embodies a program of instructions executable by the computer to perform a method to use a System-on-Chip (SOC) interconnection apparatus, said method comprising:

receiving a request from one of one or more requestors over a requestor connection port coupled to said one requestor and to an internal switching fabric;

determining which one of one or more addressable targets is the designated target using an internal system memory map; and

routing said request to said designated target over a target connection port coupled to said internal switching fabric, wherein said request routed to said designated

target further comprises a registered, point-to-point signal having a plurality of pipeline stages;

wherein said internal switching fabric, said one or more requestors, and said one or more addressable targets are all included on a single semiconductor integrated circuit, wherein each said addressable target has a unique address space and further comprises one or more of the following: resident memory, a memory controller for resident or off-chip memory, an addressable bridge to a device, an addressable bridge to a system, or an addressable bridge to a subsystem, and wherein said internal switching fabric routes signals between said requestors and said addressable targets and further comprises one or more memory arbiters and one or more decoder/router elements that receive said request from a requestor;

wherein one of said one or more decoder/router elements further comprises one of the following:

a decoder/router element that routes requests to all of said one or more addressable targets using an internal system memory map that includes unique address space information for all of said one or more addressable targets;

a decoder/router element that routes requests to less than all of said one or more addressable targets using an internal system memory map that includes unique address space information for all of said one or more addressable targets; or

a decoder/router element that routes requests to less than all of said one or more addressable targets using an internal system memory map that includes unique

address space information for less than all of said one or more addressable targets; and

wherein one of said one or more requestors and one of said one or more addressable targets together further comprise a single device having an independently accessible requestor port and an independently accessible target port; or

one of said one or more addressable targets further comprises a single device having two independently accessible target ports.